AMENDMENTS TO THE SPECIFICATION

Please amend the specification as follows:

Page 11, line 9 has been amended as follows:

Figs 11A and 11B show the arrangement of a normal ~~program~~ memory cell and a program cell, respectively.

Page 21, paragraph beginning at line 18 has been amended as follows:

Column selection lines CSL1 to ~~CLSm~~ CSLm for selecting a column are provided corresponding to the memory cell columns. In data write operation and data read operation, column decoder 25 activates one of column selection lines CSL1 to ~~CLSm~~ CSLm to the selected state (H level) according to the decode result of column address CA, that is, the column selection result.

Page 28, paragraph beginning at line 33 has been amended as follows:

Current sense amplifier 110 includes P-channel MOS transistors 111, 112 and N-channel MOS ~~transistor~~ transistors 113, 114. P-channel MOS transistor 111 and N-channel MOS transistor 113 are connected in series between power supply voltage Vcc1 and program cell PRC1. P-channel MOS transistor 112 and N-channel MOS transistor 114 are connected in series between power supply voltage Vcc1 and reference resistor 115. Program cell PRC1 is coupled between N-channel MOS transistor 113 and ground voltage Vss. Reference resistor 115 is connected between N-channel MOS transistor 114 and ground voltage Vss.

Page 41, paragraph beginning on line 17 has been amended as follows:

Referring to Fig. 17, a monitor terminal 4b is further provided in the second embodiment. Monitor terminal ~~5b~~ 4b is provided in order to monitor from the outside the redundant determination result that is obtained in redundant control circuit 105 based on the defective addresses programmed in program circuit 100.

Page 43, paragraph beginning on line 10 has been amended as follows:

As described before, in program data write operation, a current is applied to program bit lines ~~BPL1~~ PBL1, PBL2 in the opposite directions regardless of the level of program data PDj.

Page 47, paragraph beginning on line 12 has been amended as follows:

Program word lines PWL1, PWL2 corresponding to the same program unit are provided in pairs. Each pair of program word lines PWL1, PWL2 is electrically coupled together at one ends by a connection 177. Connection 177 is formed from a metal wiring or the like. The other end of one program word line PWL1 is connected to power supply voltage Vcc2 through selection transistor 170. The other end of the other program word line PWL2 is connected to ground voltage Vss. In response to activation of a program signal /PRG applied to ~~selected~~ selection transistor 170, a program current Ip(P) of a fixed direction is supplied to program word lines PWL1, PWL2 as a reciprocating current. As a result, a program magnetic field of the hard-axis direction can be applied to each magneto-resistance element.

Page 52, paragraph beginning on line 17 has been amended as follows:

With the above structure, even when the bias voltage applied across both ends of each program cell is the same as that applied across both ends of each memory cell, the difference in passing ~~current~~ currents caused by the difference in magnetization direction (that is, by the difference in storage data level) is greater in the program cells than in the memory cells. As a result, a read operation margin of the program cells is greater than that of memory cells MC, thereby enabling the program registers to have higher reliability than that of the memory cells for normal data storage.